

REMARKS

This Amendment takes into consideration the issues outstanding from the final Office Action dated October 26, 2004. Applicants respectfully request favorable reconsideration of this application in view of the amendments and remarks presented herein.

Claims 3-5 and 8-14 have been canceled without prejudice or disclaimer in order to reduce the issues. Applicants reserve the right to present these claims for future prosecution in one, or more, continuation applications. Accordingly, Claims 1, 2, 6, and 7 are pending for further consideration, with Claims 1 and 2 being independent.

In the final Office Action, Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kume in view of Kakiage. Claim 2 was rejected under 35 U.S.C. §102(b) as being anticipated by Kume et al.

Without acceding to the rejections under 35 U.S.C. §§ 102 and 103, Claims 1, 2, 6 and 7 have been amended to more clearly recite certain distinctive features of the invention. Applicants respectfully submit that the rejections under §§ 102 and 103 are inappropriate, at least insofar as considered vis-à-vis the claims as now presented.

Claim 1 is directed to a microprocessor and recites, *inter alia*, a first clock terminal to supply a first clock signal to a first external device, a second clock terminal to

supply a second clock signal, having a different frequency from the first clock signal, to a second external device, the first and second clock signals being output from the microprocessor to the first and second external devices, respectively, in parallel.

Kume, directed to a data processor, fails to teach or suggest these features. Rather, Kume discloses that clock output selector switch 20 selects one of the clock frequencies output by clock generator 30 based on data in control register 14, and then supplies this *single clock frequency* outside the processor via signal line 21. See, e.g., Abstract; Paragraph 0024; FIGS. 1 and 2.

Kakiage, directed to a bus controller, also fails to teach or suggest the aforementioned features. Instead, Kakiage discloses that synchronous clock selecting signal 110 indicates whether external clock signal 100 or internal clock signal 101 should be used by external access controlling signal generator 8 to generate bus cycle signal 111. Controlling circuit 6 then receives, *inter alia*, bus cycle signal 111 and generates address controlling signal 114 and data controlling signal 115 for controlling external address bus interface section 10 and external data bus interface section 11, respectively. See, e.g., Col. 8, lines 6-18; Col. 9, lines 1-36; FIGS. 1 and 3.

Claim 1 thus distinguishes patentably from Kume and Kakiage, at least in view of the deficiencies of the references noted above.

Moreover, none of the remaining references, taken either singly or in combination, teaches or suggests these features.

Claim 2 is directed to a microprocessor and recites, *inter alia*, a first clock signal having a predetermined frequency different from that of a second clock signal, and first and second external clock output terminals that output the first and second clock signals, respectively, in parallel. As discussed above, Kume fails to teach or suggest these features, and discloses that clock output selector switch 20 selects and outputs a *single clock frequency* via signal line 21. Claim 2 therefore distinguishes patentably from Kume on at least this basis.

Accordingly, in view of the amendments presented herein, and for the reasons explained in the preceding remarks, Applicants respectfully request that the outstanding rejections be withdrawn and that this application now be passed to issue.

A Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is

required in connection with the filing of this paper and has not been requested separately, then such extension is hereby requested.

Respectfully submitted,

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